CLAIM AMENDMENTS

Please cancel claims 40-43 without prejudice or disclaimer.

Please amend claims 8, 33, and 37, as follows.

1. (Previously Presented) An apparatus, comprising:

an integrated circuit having:

a set of voltage generators to generate a set of direct current (DC) voltages;

a set of sense amplifiers coupled to compare an externally supplied reference voltage with the set of DC voltages; and

a boundary scan register coupled to each sense amplifier in the set of sense amplifiers to interpret the comparison of the externally supplied reference voltage and the set of DC voltages.

2. (Original) The integrated circuit of claim 1 wherein the set of voltage generators is responsive to a set of configuration bits to determine the set of DC voltages.

3. (Original) The integrated circuit of claim 2, further comprising a set of switches coupled between the set of voltage generators and the set of sense amplifiers to enable the set of DC voltages to be applied to the non-inverting input of each sense amplifier in the set of sense amplifiers.

4. (Original) The integrated circuit of claim 2, wherein each voltage generator in the set of voltage generators is a digital-to-analog converter.

5. (Previously Presented) The integrated circuit of claim 3, further comprising second logic to open and close a set of switches to connect the set of DC voltages to the non-inverting inputs of the set of sense amplifiers.

6. (Original) The integrated circuit of claim 5, wherein the second logic comprises a boundary-scan register.

7. (Original) The integrated circuit of claim 5, wherein the second logic comprises an input/output loop back pattern generator.

8. (Currently Amended) A system, comprising:

an integrated circuit having a set of voltage generators to generate a set of direct current (DC) voltages, a set of sense amplifiers coupled to compare a reference voltage with the set of DC voltages, and a boundary scan register coupled to each sense amplifier in the set of sense amplifiers to interpret the comparison of the reference voltage and the set of DC voltages, the set of voltage generators to incrementally increase and/or decrease the set of DC voltages to determine a set of trip points for the set of sense amplifiers, the set of trip points being associated with a logical one input voltage level and/or a logical zero input voltage level; and

a structural tester coupled to the integrated circuit to apply a reference voltage to the inverting input of each sense amplifier in the set of sense amplifiers.

9. (Original) The system of claim 8, wherein the set of voltage generators is responsive to a set of configuration bits to determine the set of DC voltages.

10. (Original) The system of claim 8, wherein the integrated circuit further comprises a set of switches coupled between the set of voltage generators and the set of sense amplifiers to enable the set of DC voltages to be applied to the non-inverting input of each sense amplifier in the set of sense amplifiers.

11. (Original) The system of claim 8, wherein each voltage generator in the set of voltage generators is a digital-to-analog converter.

Claims 12-25. (Canceled).

26. (Previously Presented) An apparatus, comprising:

an integrated circuit device having:

a set of input pins;

levels generating circuitry coupled to a subset of the input pins;

logic to apply a set of configuration bits to the levels generating circuitry to enable concurrent input levels testing or parallel input levels testing of the set of input pins using the subset of input pins;

a set of voltage generators to generate a set of direct current (DC) voltages;

a set of sense amplifiers coupled to compare an external reference voltage with the set of DC voltages; and

logic coupled to each sense amplifier in the set of sense amplifiers to interpret the comparison of the external reference voltage and the set of DC voltages.

27. (Canceled)

28. (Previously Presented) The apparatus of claim 26, further comprising a set of switches coupled between the set of voltage generators and the set of sense amplifiers to enable the set of DC voltages to be applied to the non-inverting input of each sense amplifier in the set of sense amplifiers.

29. (Previously Presented) The integrated circuit of claim 26, wherein each voltage generator in the set of voltage generators is a digital-to-analog converter.

30. (Previously Presented) A method, comprising:

testing at least one integrated circuit device having a first number of input pins and levels generating circuitry coupled to at least some of the first number of input pins by:

receiving a set of configuration bits at the levels generating circuitry;

receiving test input levels at a second smaller number of input pins to enable parallel input levels testing of the first number of input pins;

generating direct current (DC) voltages;

comparing an external reference voltage with the set of DC voltages; and

interpreting the comparison of the external reference voltage and the set of DC voltages.

31. (Canceled)

32. (Previously Presented) The method of claim 30, wherein receiving a set of configuration bits at a levels generating circuitry comprises receiving a set of configuration bits at digital-to-analog converters.

33. (Currently Amended) A system, comprising:

an integrated circuit having a set of voltage generators to generate a set of direct current (DC) voltages, a set of sense amplifiers coupled to compare a reference voltage with the set of DC voltages, and input/output loop back compare circuitry coupled to each sense amplifier in the set of sense amplifiers to interpret the comparison of the reference voltage and the set of DC voltages, the set of voltage generators to incrementally increase and/or decrease the set of DC voltages to determine a set of trip points for the set of sense amplifiers, the set of trip points being associated with a logical one input voltage level and/or a logical zero input voltage level; and

a structural tester coupled to the integrated circuit to apply a reference voltage to the inverting input of each sense amplifier in the set of sense amplifiers.

34. (Previously Presented) The system of claim 33, wherein the set of voltage generators is responsive to a set of configuration bits to determine the set of DC voltages.

35. (Previously Presented) The system of claim 33, wherein the integrated circuit further comprises a set of switches coupled between the set of voltage generators and the set of sense amplifiers to enable the set of DC voltages to be applied to the non-inverting input of each sense amplifier in the set of sense amplifiers.

36. (Previously Presented) The system of claim 33, wherein each voltage generator in the set of voltage generators is a digital-to-analog converter.

37. (Currently Amended) A system, comprising:

an integrated circuit having a set of voltage generators to generate a set of direct current (DC) voltages, a set of sense amplifiers coupled to compare a reference voltage with the set of DC voltages, and logic coupled to each sense amplifier in the set of sense amplifiers to interpret the comparison of the reference voltage and the set of DC voltages, the set of voltage generators to incrementally increase and/or decrease the set of DC voltages to determine a set of trip points for the set of sense amplifiers, the set of trip points being associated with a logical one input voltage level and/or a logical zero input voltage level;

a structural tester coupled to the integrated circuit to apply a reference voltage to the inverting input of each sense amplifier in the set of sense amplifiers; and

a set of switches coupled between the set of voltage generators and the set of sense amplifiers to enable the set of DC voltages to be applied to the non-inverting input of each sense amplifier in the set of sense amplifiers, and wherein the integrated circuit further comprises second logic coupled to open and close the set of switches.

38. (Previously Presented) The system of claim 37, wherein the second logic comprises a boundary-scan register.

39. (Previously Presented) The system of claim 37, wherein the second logic comprises an input/output loop back pattern generator.

Claims 40-43. (Canceled).